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EXAMINER
FAHERTY, COREY S

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,421	LEIJTEN, JEROEN ANTON JOHAN	
	Examiner	Art Unit	
	Corey S. Faherty	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the reply filed on 06/04/2009.

2. Claims 1-11, 13 and 15-17 are pending in the application and have been examined.

3. Claim 17 recites the limitation "an wherein" and should recite "and wherein".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. **Claims 1-3, 5-7, 9, 13 and 15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Downing (U.S. Patent 3,781,810).

7. Regarding claims 1 and 13, Downing discloses a data processor comprising:

one or more functional units arranged to provide an internal processor [Fig. 2],

one or more register files [Fig. 2; computer registers],

a data memory facility having a multibit access port facility [Fig. 2],

a snapshot buffer, differing from the one or more register files [auxiliary registers], which during handling of an interrupt condition accommodates saving, by copying from the one or more register files to respective snapshot buffer elements, state information of various processor state elements, including state information from the internal processor [col. 3, lines 25-27], and

a controller means arranged to save, upon occurrence of a subsequent interrupt condition during handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility having the multibit access port facility [col. 4, lines 5-10; col. 2, lines 12-17].

Downing does not explicitly disclose that the system is pipelined. However, the use and benefits of pipelining are notoriously well known in the art, and the use of the techniques described by Downing in a pipelined processor would therefore have been obvious to a person having skill in the art.

8. Regarding claim 2, Downing discloses the data processor as claimed in Claim 1, wherein said controller means are arranged to retrieve the saved contents of said snapshot buffer elements from said data memory facility through said multibit access port facility back into said snapshot buffer elements upon completing the handling of the actual interrupt condition [col. 4, lines 55-58; col. 2, lines 12-17].

9. Regarding claim 3, Downing discloses the data processor as claimed in Claim 2, wherein said controller means are arranged to restore the retrieved saved state information of various processor state elements allowing said data processor to proceed with handling one of an earlier uncompleted interrupt or continuing a main thread of the processing [col. 4, lines 28-31; col. 5, lines 21-24; col. 2, lines 12-17].

10. Regarding claim 5, Downing discloses the data processor as claimed in Claim 1, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility [col. 3, lines 44-53].

11. Regarding claim 6, Downing discloses the data processor as claimed in Claim 1, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility [col. 4, lines 40-58].

12. Regarding claim 7, Downing does not explicitly disclose that the data memory facility is operated as a stack. However, the practice and benefits of operating a data memory facility as a stack in the field of context preservation are well known in the art (see the Cohen reference cited in rejections of previous actions, for instance). Such operation would therefore have been obvious in the system of Downing.

13. Regarding claim 9, Downing discloses the data processor as claimed in Claim 7, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility [col. 4, lines 40-58], wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility [col. 3, lines 44-53], and wherein write and read operations in said stack are executed at mutually exclusive instants in time [col. 4, lines 40-58; col. 3, lines 44-53] under control of a stack pointer [obvious as described in rejection of claim 7].

14. Regarding claim 15, Downing does not explicitly disclose saving the processor state elements to the snapshot buffer in a single clock cycle. However, the concept and advantages of performing a data operation in a single clock cycle in a processing system are well known in the computer arts, and it therefore would have been obvious to one of ordinary skill in the art to do so.

15. Regarding claim 16, Downing does not explicitly disclose restoring the processor state elements from the snapshot buffer in a single clock cycle. However, the concept and advantages of performing a data operation in a single clock cycle in a processing system are well known in the computer arts, and it therefore would have been obvious to one of ordinary skill in the art to do so.

16. Regarding claim 17, Downing discloses the data processing facility of Claim 1, wherein the controller means saves, upon occurrence of the subsequent interrupt condition during the handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility [col. 4, lines 10-14] using a stack pointer [obvious as described in rejection of claim 7], and wherein no additional instruction bits are required for addressing the snapshot buffer elements [col. 4, lines 5-10].

17. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Downing as applied to claim 1 above, and further in view of Petolino, Jr. et al. (U.S. Patent 5,958,041), referenced from here forward as Petolino.

18. Regarding claim 4, Downing discloses that the state to be saved during interrupt processing includes data that is associated with the currently executing code [abstract], but does not explicitly disclose that this data includes latency data of current operations.

Petolino discloses a processor in which each load instruction has an associated latency prediction bit that is used to predict the proper latency period between the issuance of a load instruction and the issuance of any dependent instructions [col. 4, lines 25-30]. The purpose of the bit is to minimize the delay necessary for executing a load instruction and any dependent instructions in a processor [col. 4, lines 16-22, 59-67; col. 5, lines 1-8].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include instruction latency data of current operations in the state that is saved during interrupt handling in the system of Downing because Downing discloses saving data that is associated with currently executing code in response to an interrupt [abstract] and Petolino discloses associating an instruction latency bit with each load instruction [col. 4, lines 25-30] for the purpose of minimizing the delay necessary for executing a load instruction and any dependent instructions in a processor [col. 4, lines 16-22, 59-67; col. 5, lines 1-8].

19. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Downing as applied to claim 7 above, and further in view of Patterson et al. (*Computer Organization & Design: The Hardware/Software Interface*), referenced from here forward as Patterson.

20. Regarding claim 8, Downing does not explicitly disclose that said stack has a stack pointer that allows multiple stack positions per snapshot. However, Downing does disclose that, during the handling of an interrupt, multiple registers are saved to the memory [col. 3, lines 44-52].

Patterson discloses a typical method for the handling of a stack memory structure in a processor [pages 134-135; Figure 3.10]. The method includes decrementing the stack pointer using a subtract instruction (sub) and using store instructions (*sw*) to push registers onto the stack. Because multiple registers are pushed onto the stack, the value of the stack pointer is decremented by a value three times the size of each register. In this way, the multiple registers are pushed onto the stack at different stack locations.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the stack pointer of Downing allow multiple stack positions per snapshot because Downing discloses that a single snapshot includes multiple registers [ol. 3, lines 44-52] and Patterson discloses a typical method for handling a memory stack in which each register that is pushed onto the stack has its own stack location [pages 134-135; Figure 3.10]. Furthermore, allowing each register to have its own stack location gives the processor more versatility in determining which registers will be saved on the stack, potentially decreasing the processing time required to perform the save operation.

21. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Downing as applied to claim 1 above, and further in view of Forsyth (U.S. Patent 5,327,566).

22. Regarding claim 10, Downing does not explicitly disclose that the snapshot buffer is constructed from shadow flip-flops for storing the snapshot information. However, as shown by Forsyth [col. 4, lines 50-66], the use and benefits (primarily, a reduction in the time required to transfer data during a context switch) of shadow storage elements in save/restore context mechanisms are well known in the art, and such operation would therefore have been obvious in the system of Downing.

23. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Downing as applied to claim 1 above, and further in view of Lang et al. (*Individual Flip-Flops with Gated Clocks for Low Power Datapaths*), referenced from here forward as Lang.

24. Regarding claim 11, Downing does not explicitly disclose that the auxiliary registers are operated at low power by clocking them only during actual taking of a snapshot.

Lang discloses a method for operating flipflops in which the flipflops are only clocked when the flipflop must change [section 1, paragraph 3]. The purpose of doing this is to reduce the energy that is consumed by the clock circuits internal to the flipflop [section 1, paragraph 3].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to clock the storage elements comprising the auxiliary registers in Downing only during actual taking of a snapshot because Lang discloses a technique in which storage elements are clocked only when the flipflop must change values [section 1, paragraph 3] and teaches that using this technique reduces the energy that is consumed by the clock circuits internal to the storage elements [section 1, paragraph 3].

Response to Arguments

25. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/Corey S Faherty/
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